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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/699,947	10/30/2000	Edmund J. Kelly	TRANS04D	8830

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IV (TRANSMETA)
C/O MURABITO, HAO & BARNES LLP
TWO NORTH MARKET STREET
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EXAMINER	
THAI, TUAN V	
ART UNIT	**PAPER NUMBER**
2185	

MAIL DATE	DELIVERY MODE
01/26/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/699,947	KELLY ET AL.	
	Examiner	Art Unit	
	Tuan V. Thai	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/12/2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,18 and 20-42* is/are pending in the application.

4a) Of the above claim(s) *2,4-17 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,18,20,21,23-26,28,30,31,34-38,41 and 42* is/are rejected.

7)☒ Claim(s) *22,27,29,32,33,39 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This action is responsive to Request for Continued Examination (RCE) filed November 12, 2009. Claims 2, 4-17 and 19 have been canceled. Claims 29-42 are newly added. Claims1, 3, 18 and 20-41 are presented for examination.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set for in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.1 14, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.1 14. Applicant's submission filed on 11/12/2009 has been entered.

3. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

4. Applicant's arguments filed November 12, 2009 with respect to the rejected claims have been fully considered but they are deemed to be mooted in view of a new ground of rejection.

Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 21, 23, 30-31 and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rozas (USPN: 6,738,893) in view of Moore et al. (USPN: 5,437,017); hereinafter Moore.

As per claims 1 and 3; Rozas discloses the invention as claimed including a system comprises means for providing an indication whether a first memory address to be written stores a target instruction for a first instruction set architecture which has been translated to at least one host instruction for a second instruction set architecture, the at least host

instruction stored at a second memory address (e.g. see column 2, lines 59 et seq.). Rozas, however does not particularly discloses the means for providing comprises a look-aside buffer including a first storage location for the first memory address, a storage position corresponding to the first memory address for storing an indication, and in responding to the indication, means for removing the at least one host instruction from the second memory address when the first memory address has been written (claim 1), or invalidating the at least one host instruction at the second memory address (claim 3) for maintaining data consistency within the system. Moore, in his teaching of method and system for maintaining TLB coherency in a multiprocessor data processing system, discloses the missing elements that are known to be required in the system of Rozas in order to arrive at Applicant's current invention wherein Moore discloses translation look-aside buffers having storing position for storing indication wherein data synchronization is implemented throughout the multiprocessor data processing system; particularly, issuing the translation lookaside buffer invalidate (TLBI) instruction at all processors within the system (claim 3) (e.g. see column 2, lines 36-37; column 3, lines 12-27; figure 5, column 8, lines 32 et seq.), wherein the removing of the at least one host instruction at the second

address is being equivalently taught as terminating the execution of all pending instructions (including host instruction) until after the TLBI instruction has been executed, or suspending execution of all pending instructions until all read and write operations within the memory queue have achieved coherency (e.g. see column 3, lines 19-27). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the translation look-aside buffers having multiple storage locations for virtual addresses and physical addresses with a first memory address, a storage position corresponding to the first memory address for storing an indication, and in responding to the indication, removing/invalidating the at least one host instruction from the second memory address when the first memory address has been written as taught by Moore for that of Rozas's system in order to arrive at Applicant's current invention. By removing and invalidating the host instruction from the second memory address, particularly when there is an update or modification of data/instruction within the system, it would prevent other processors or I/O units from executing stale or out-of-date instruction/data; thereby data coherency can be uniformly maintained, therefore being greatly advantageous.

As per claim 21, the further limitation of the indication comprises a first bit value associated with each of the storage locations in the look-aside buffer; PTE translator 42 and BAT translator 44 (e.g. see Moore's figures 1-3; column 2, lines 7 et seq.; column 4, lines 19 et seq.).

As per claim 23, Rozas further discloses the host processor is a very long instruction word processor and wherein the target instruction set architecture comprises x86 instructions (e.g. column 4, lines 11 et seq.).

As per claim 30, see arguments with respect to claim 1. Claim 30 encompasses the same scope of invention as to that of claim 1, the claim is therefore rejected for the same reason as being set forth above.

As per claim 31, Moore discloses the storage position is associated with a storage location for the first memory address in a look-aside buffer (e.g. PTE translator 42 and BAT translator 44 (e.g. see Moore's figures 1-3; column 2, lines 7 et seq.);, wherein the look-aside buffer comprises a plurality of storage locations for virtual addresses and associated physical addresses column 4, lines 19 et seq.).

As per claim 37, see arguments with respect to claim 1. Claim 37 encompasses the same scope of invention as to that of claim 1, the claim is therefore rejected for the same reason as

being set forth above. Noting that Rozas discloses the embedded memory and the VLIW processor (e.g. see column 3, lines 50 et seq.).

As per claim 38, the further limitation of the indication comprises a first bit value e.g. PTE translator 42 and BAT translator 44 associated with TLB 40 (e.g. see Moore's figures 1-3; column 2, lines 7 et seq.; column 4, lines 19 et seq.).

Allowable subject matter

7. Claims 22, 24, 32, 34, 39 and 41-42 are objected to as being dependent upon a rejected based claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 18 is allowed. Claims 20, 25-28, 29, 33, 35-36 and 40 are also allowable since it is depended on the indicated allowable claims 18, 22, 24, 32, 34, 39.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V.

Thai whose telephone number is (571)-272-41287. The examiner can normally be reached from 6:30 A.M. to 3:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571)-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-9300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/January 18, 2010

/Tuan V. Thai/
Primary Examiner, Art Unit 2185